Amendments to the Claims:

Listing of Claims:

Claim 1 (currently amended): A method for determining whether a memory is defected or has integrity under a plurality of operating environments comprising:

setting a plurality of operating environments respectively corresponding to variations in a condition to be tested;

repeatedly testing the same memory having defective sections under each of the plurality of operating environments;

recording a result of the testing step for each of the plurality of operating environments; and

comparing the recorded results for each of the plurality of operating environments, wherein if the results are the same for each of the plurality of operating environments then the memory is determined to have integrity and if the results are different for at least two of the plurality of operating environments then the memory is determined to be defected.

Claim 2 (previously presented): The method of claim 1, wherein the testing step further comprises:

performing a built-in self test (BIST) on the memory under each of the plurality of operating environments.

Claim 3 (previously presented): The method of claim 2 further comprising:

marking a status record memory according to the BIST, wherein the status record memory corresponds to the memory; and

recording the content of the status record memory for each of the plurality of operating environments.

Claim 4 (original): The method in claim 1 wherein the condition to be tested is a variance

in supply voltage.

Claim 5 (original): The method in claim 1 wherein the condition to be tested is a variance in temperature.

Claim 6 (previously presented): The method of claim 1 wherein the testing step further comprises:
detecting information concerning defects in the memory; and
counting the number of defects in the memory under each of the plurality of operating environments.

Claim 7 (previously presented): The method in claim 6 wherein the recording step further comprises:
storing the number of defects detected in the memory.

Claim 8 (previously presented): The method in claim 7 wherein the comparing step further comprises:
accessing the stored number of defects to determine if the numbers of defects detected in the memory under each of the plurality of operating environments are equal to one another;
wherein if the numbers of defects detected in the memory under each of the plurality of operating environments are equal to one another then the memory is determined to have integrity.

Claim 9 (previously presented): The method in claim 6 wherein the recording step further comprises:
recording and storing the position of each defect detected in the memory under each of the plurality of operating environments.

Claim 10 (previously presented): The method in claim 9 wherein the comparing step further comprises:

determining if the positions of defects of the memory under each of the plurality of operating are the same as one another.

Claim 11 (currently amended): A method for determining whether a memory is defected or has integrity, comprising:

testing the memory having defective sections under a first operating environment corresponding to a condition to be tested;

recording a first result of the testing step under the first operating environment;

testing the memory having defective sections under a second operating environment, wherein the second operating environment corresponds to a variation of the condition to be tested in the first operating environment;

recording a second result of the testing step under the second operating environment; and

comparing the first result with the second result, wherein if the first result is equal to the second result then the memory is determined to have integrity and if the first result is different from the second result then the memory is determined to be defected.

Claim 12 (previously presented): The method of claim 11 wherein the testing steps further comprise:

performing a built-in self test (BIST) on the memory.

Claim 13 (original): The method of claim 12 further comprising:

marking a status record memory according to the BIST, wherein the status record memory corresponds to the memory; and

recording the content of the status record memory for the current operating environment.

Claim 14 (previously presented): The method in claim 11 wherein the condition to be tested in the first and the second operating environment is supply voltage.

Claim 15 (previously presented): The method in claim 11 wherein the condition to be tested in the first and the second operating environment is temperature.

Claim 16 (previously presented): The method in claim 11 further comprising:
determining whether the first and second results are consistent or inconsistent with one another.

Claim 17 (previously presented): The method in claim 11 wherein the first result comprises information of defect locations in the memory corresponding to the first operating environment and the second result comprises information of defect locations in the memory corresponding to the second operating environment.

Claim 18 (currently amended): A method for determining integrity of a memory with sections that are defective, the method comprising:
repeatedly testing the memory <u>having defective sections</u> under a plurality of operating environments respectively corresponding to a given condition to be tested;
recording a result of the testing step for each of the plurality of operating environments;
comparing the results; and
determining whether the results are consistent or inconsistent with one another;

wherein the results correspond to the given condition, and if ~~they~~ the results are consistent with one another the memory is determined to have integrity and if the results are inconsistent with one another then the memory is determined to be defected.

Claim 19 (previously presented): The method in claim 18 wherein the first result comprises information regarding the number of defective sections in the memory corresponding to the first operating environment and the second result comprises information regarding the number of defective sections in the memory corresponding to the second operating environment.

Claim 20 (previously presented): The method in claim 18 wherein the first result comprises information regarding locations of defective sections in the memory corresponding to the first operating environment and the second result comprises information regarding locations of defective sections in the memory corresponding to the second operating environment.

Claim 21 (new): A method for determining whether a memory is defected or has integrity under a plurality of operating environments comprising:

setting a plurality of operating environments respectively corresponding to variations in a condition to be tested;

repeatedly testing the same memory under each of the plurality of operating environments;

recording a result of the testing step for each of the plurality of operating environments; and

comparing the recorded results for each of the plurality of operating environments, wherein if the results are the same for each of the plurality of operating environments then the memory is determined to have integrity

and if the results are different for at least two of the plurality of operating environments then the memory is determined to be defected.

Claim 22 (new): The method of claim 21, wherein the testing step further comprises:
performing a built-in self test (BIST) on the memory under each of the plurality of operating environments.

Claim 23 (new): The method of claim 22 further comprising:
marking a status record memory according to the BIST, wherein the status record memory corresponds to the memory; and
recording the content of the status record memory for each of the plurality of operating environments.

Claim 24 (new): The method in claim 21 wherein the condition to be tested is a variance in supply voltage.

Claim 25 (new): The method in claim 21 wherein the condition to be tested is a variance in temperature.

Claim 26 (new): The method of claim 21 wherein the testing step further comprises:
detecting information concerning defects in the memory; and
counting the number of defects in the memory under each of the plurality of operating environments.

Claim 27 (new): The method in claim 26 wherein the recording step further comprises:
storing the number of defects detected in the memory.

Claim 28 (new): The method in claim 27 wherein the comparing step further comprises:

accessing the stored number of defects to determine if the numbers of defects detected in the memory under each of the plurality of operating environments are equal to one another;

wherein if the numbers of defects detected in the memory under each of the plurality of operating environments are equal to one another then the memory is determined to have integrity.

Claim 29 (new): The method in claim 26 wherein the recording step further comprises:

recording and storing the position of each defect detected in the memory under each of the plurality of operating environments.

Claim 30 (new): The method in claim 29 wherein the comparing step further comprises:

determining if the positions of defects of the memory under each of the plurality of operating are the same as one another.